LISTING OF CLAIMS

1-9. (Canceled)

10. (Original) A method of forming a shallow trench isolation region in a layer of semiconductor material, comprising:

forming a trench in the layer of semiconductor material, the trench having sidewalls and a bottom;

forming a layer of high-K material, the layer of high-K material conforming to the sidewalls and the bottom of the trench to line the trench with a high-K liner; and

filling the high-K material lined trench with an isolating material.

11. (Original) The method according to claim 10, further comprising forming a semiconductor device using an active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, wherein the high-K material has a compressive stress to compress the active region, the compressive stress effective to enhance electron mobility within the active region.

12. (Original) The method according to claim 11, wherein the semiconductor device is an NMOS device.

13. (Currently amended) The method according to claim 10, further comprising forming a semiconductor device using an active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, wherein the high-K material has a tensile stress to strain the active region, the tensile stress effective to enhance hole mobility within the active region.

14. (Original) The method according to claim 13, wherein the semiconductor device is a PMOS device.

15. (Original) The method according to claim 10, wherein the fill section is composed of one or more materials selected from silicon oxide, silicon nitride, polysilicon and mixtures thereof.

16. (Original) The method according to claim 15, wherein the fill section is deposited using chemical vapor deposition (CVD).

17. (Original) The method according to claim 10, wherein the layer of semiconductor material is a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

18. (Original) The method according to claim 17, wherein the bottom of the trench is defined by the insulating layer.

19. (New) The method according to claim 10, wherein the layer of high-K material has a relative permittivity (K) of about 10 or more.

20. (New) The method according to claim 10, wherein the layer of high-K material has a relative permittivity (K) of about 20 or more.

21. (New) A method of enhancing carrier mobility in a semiconductor active region of a semiconductor device, comprising:

providing a layer of semiconductor material;

providing a trench isolation region in the layer of semiconductor region that defines placement of the active region, the trench isolation region defined by sidewalls and a bottom and includes:

a liner made from a material having a relative permittivity (K) of about 10 or more, the liner conforming to the sidewalls and bottom; and

a fill section made from isolating material that is disposed within and conforms to the liner; and

exerting a mechanical stress on the active region with the liner to enhance carrier mobility within the active region.

22. (New) The method according to claim 21, further comprising forming the semiconductor device using an active region and wherein the liner has a compressive stress to compress the active region, the compressive stress effective to enhance electron mobility within the active region.

23. (New) The method according to claim 22, wherein the semiconductor device is an NMOS device.

24. (New) The method according to claim 21, further comprising forming the semiconductor device using an active region and wherein the liner has a tensile stress to strain the active region, the tensile stress effective to enhance hole mobility within the active region.

25. (New) The method according to claim 24, wherein the semiconductor device is a PMOS device.

26. (New) The method according to claim 21, wherein the fill section is composed of one or more materials selected from silicon oxide, silicon nitride, polysilicon and mixtures thereof.

27. (New) The method according to claim 26, wherein the fill section is deposited using chemical vapor deposition (CVD).

28. (New) The method according to claim 21, wherein the layer of semiconductor material is a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

29. (New) The method according to claim 28, wherein the bottom of the trench is defined by the insulating layer.

30. (New) The method according to claim 21, wherein the liner has a relative permittivity (K) of about 20 or more.

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